Previous Doc Next Doc Go to Doc#
First Hit Fwd Refs

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L10: Entry 1 of 1 File: USPT Aug 6, 1996

DOCUMENT-IDENTIFIER: US 5544319 A
TITLE: Fiber optic memory coupling system with converter transmitting and receiving bus data in parallel fashion

Abstract Text (1):
A system for coupling sets of plurality of nodes that are memory coupled to pass write only data memory to memory via a data link that further includes an optical fiber controller coupled to each data link. Each controller is interconnected through fiber for high speed data transfers from one set of nodes to another. The controller is capable of connection implementing three and four cable interfaces. The data is transmitted through the fiber serially but the controller is adapted to receive parallel data and convert to serial form and vice versa.

Drawing Description Text (3):
FIG. 2 illustrates the fiber to memory coupled system controller (FMC);

Detailed Description Text (2):
This invention relates to a high speed data interface system using fiber optic memory interconnection as shown in FIG. 1. This interface system connects memory coupled systems over distances up to 10 kilometers. Each memory coupled system comprises a data link or memory coupling bus 5 to which up to eight nodes 6 are coupled each comprising a processor, I/O, a two or more ported memory and a processor to memory bus. Write/read sense controllers couple the busses and the memory so writes only are sensed and reflected to the memories of other nodes without CPU intervention. This is described in detail in the patent and application noted above, both of which are here incorporated by reference. The bus 5 of each memory coupled system is connected to a fiber-to-memory coupling system controller (FMC) 1. Each FMC has both an input and output port for connection with another FMC. The input port 2 is for receiving transmitted data from another memory coupled system and the output port 3 is for transmitting data to another memory coupled system. The transmission of the data is through fiber optic cables 4.

Detailed Description Text (18):
Support for burst request mode in the FMC is enabled or disabled via a configuration programming command. Only one FMC on a given MC bus can have burst request mode enabled but at least one FMC in every FMC-to-FMC link must have the mode enabled to ensure reliable operation. Note that enabling burst request mode in the FMC only means that the FMC is able to drive BURST REQUEST on the bus. For burst request mode to be useful, the four cable MCS-II environment with Memory Coupling Controllers (MCC's) as the bus arbiter/terminators is required. MCC's provide bus termination and arbitration in a conventional manner as known from the previously noted patent and application and are sometimes referred to as reflective memory controllers.

Previous Doc Next Doc Go to Doc#

Hit List

First Hit | Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 1 of 1 returned.

☐ 1. Document ID: US 5544319 A

L4: Entry 1 of 1 File: USPT Aug 6, 1996

DOCUMENT-IDENTIFIER: US 5544319 A
TITLE: Fiber optic memory coupling system with converter transmitting and receiving bus data in parallel fashion and diagnostic data in serial fashion

Abstract Text (1):
A system for coupling sets of plurality of nodes that are memory coupled to pass write only data memory to memory via a data link that further includes an optical fiber controller coupled to each data link. Each controller is interconnected through fiber for high speed data transfers from one set of nodes to another. The controller is capable of connection implementing three and four cable interfaces. The data is transmitted through the fiber serially but the controller is adapted to receive parallel data and convert to serial form and vice versa.

Drawing Description Text (12):
FIG. 11 illustrates a parallel/serial latch used in the present invention;

Detailed Description Text (36):
An important feature of the FMC design, particularly from a diagnostic perspective, is that the latches in each quadrant can be accessed in both a parallel and serial fashion. During normal operation of the FMC, data moves through the latches using the parallel interface. The alternate serial interface allows the microprocessor on the FMC to shift data serially into and out of the latches.

Detailed Description Text (49):
FIG. 11 shows a block diagram of the AMD 29818 latch used to implement the MC input and output latches 9 and 10 and the Rx latches 15 and 17 and Tx latches 18 and 20 on the FMC. In the FMC design, the normal data path through these latches is the parallel one from the D input through the pipeline register 29 to the Q output. The alternate serial path is accessible by the FMC microprocessor and is primarily used for diagnostic purposes. Note that the mux 30 (which is controlled by the MODE signal) allows either the contents of the shadow register 31 or the D input to serve as the input for the pipeline register 29. Also, note that the output of the pipeline register 29 is feed back into the shadow register 31. Thus, with appropriate hardware control, data can enter the latch in serial and exit in parallel or enter parallel and exit in serial.

Detailed Description Text (51):
In the FOMCS architecture, the high speed serial link is implemented with a transmit/receive pair of Gazelle Hot Rod chips. The Gazelle Hot Rod transmitter chip converts 40-bit parallel data into serial data that is transmitted over a fiber or coax link. At the remote end of the link, the data is reconverted to the original parallel data by a Hot Rod receiver chip. Over this link, the FMCs exchange information in the form of 80-bit packets. The Gazelle transmitter sends

each 80-bit packet as two 40-bit data frames. When no packet is available to send, the transmitter sends sync frames to maintain link synchronization.

CLAIMS:

1. A system comprising:

a first and second set of plurality of nodes;

a first bus associated with and connecting said first set of plurality nodes;

a second bus associated with and connecting said second set of plurality of nodes;

each node except one of each of said first and second sets of plurality of nodes including a processing unit, a memory, a bus coupled to the processing unit and memory, and a sensor means for sensing a write from the processing unit to the memory and for transmitting the sensed write including data and an address to which said data is being written on said associated bus without intervention of the processing unit;

fiber optic means for optically transmitting data and associated addresses from one excepted node to the other excepted node;

the excepted node of the first set of plurality of nodes including first converter means connected to the first bus for (1) receiving data and associated addresses on said first bus in a parallel fashion, (2) converting said data to corresponding optical signals, (3) transmitting said optical signals via said fiber optic means, (4) receiving optical signals from said fiber optic means in a serial fashion, and (5) transmitting the optical signals received from said fiber optic means onto said first bus, said first converter means including latches receiving and outputting data from said first bus or said fiber optic means in a parallel fashion and receiving and outputting diagnostic data in a serial fashion;

the excepted node of the second set of plurality of nodes including second converter means connected to the second bus for (1) receiving data and associated addresses on said second bus in a parallel fashion, (2) converting said data to corresponding optical signals, (3) transmitting said optical signals via said fiber optic means, (4) receiving optical signals from said fiber optic means in a serial fashion, and (5) transmitting the optical signals received from said fiber optic means onto said second bus, said second converter means including latches receiving and outputting data from said second bus or said fiber optic means in a parallel fashion and receiving and outputting diagnostic data in a serial fashion; and

both said first and second converter means including selection means for accepting for transmission only data having preselected associated addresses.

5. A system for connecting memory coupled systems, comprising:

a plurality of nodes;

a first data bus connecting a first group of said plurality of nodes;

a second data bus connecting a second group of said plurality of nodes;

one of said plurality of nodes of the first group including first converter means for converting signals on the first data bus to optical signals and for transmitting same;

one of said plurality of nodes of the second group including second converter means for converting signals on the second data bus to optical signals and for

transmitting same;

first fiber optic means for carrying transmitted data from the first converter means to the second converter means;

second fiber optic means for carrying transmitted data from the second converter means to the first converter means;

the first and second converter means each comprising:

input latch means for receiving data from a respective data bus and having inputs and outputs accessible both in a parallel fashion and a serial fashion;

hit and translation RAM means connected to the input latch means for determining the destination of data received from the data bus;

first micro-interface means connected to the input latch means for controlling the hit and translation RAM means;

transmission FIFO means connected to the input latch means for latching the data received from the data bus;

error detection means for determining if an error exists in the data in the transmission FIFO means;

first and second transmission latches connected to the transmission FIFO means, each of said transmission latches having inputs and outputs accessible both in a parallel fashion and in a serial fashion;

transmitter means connected to the first and second transmission latches for transmitting the data to another converter means;

receiver means for receiving data transmitted from another converter means;

first and second receiver latches for latching the received data, each of said receiver latches having inputs and outputs accessible both in a parallel fashion and in a serial fashion;

error detection means connected to the first and second latch means for checking if an error exists in the received data;

second micro-interface means for testing the received data if the check by the error detection means fails;

receive FIFO means connected to the first and second receive latch means for holding the received data after checking by the error detection means;

output latch means for transmitting the received data to the respective data bus and having inputs and outputs accessible both in a serial fashion and in a parallel fashion.

Term	Documents
SERIAL	196207
SERIALS	144
PARALLEL	1270750
PARALLELS	9397
(1 AND (SERIAL WITH PARALLEL)).USPT.	1
(L1 AND (SERIAL WITH PARALLEL)).USPT.	1

Display Format: KWIC Change Format

Previous Page Next Page Go to Doc#

Corrected

Hit List

Search Results - Record(s) 1 through 1 of 1 returned.

☐ 1. Document ID: US 5544319 A

L5: Entry 1 of 1 File: USPT Aug 6, 1996

DOCUMENT-IDENTIFIER: US 5544319 A
TITLE: Fiber optic memory coupling system with converter transmitting and receiving bus data in parallel fashion and diagnostic data in serial fashion

Abstract Text (1):
A system for coupling sets of plurality of nodes that are memory coupled to pass write only data memory to memory via a data link that further includes an optical fiber controller coupled to each data link. Each controller is interconnected through fiber for high speed data transfers from one set of nodes to another. The controller is capable of connection implementing three and four cable interfaces. The data is transmitted through the fiber serially but the controller is adapted to receive parallel data and convert to serial form and vice versa.

Detailed Description Text (51):
In the FOMCS architecture, the high speed serial link is implemented with a transmit/receive pair of Gazelle Hot Rod chips. The Gazelle Hot Rod transmitter chip converts 40-bit parallel data into serial data that is transmitted over a fiber or coax link. At the remote end of the link, the data is reconverted to the original parallel data by a Hot Rod receiver chip. Over this link, the FMCs exchange information in the form of 80-bit packets. The Gazelle transmitter sends each 80-bit packet as two 40-bit data frames. When no packet is available to send, the transmitter sends sync frames to maintain link synchronization.

CLAIMS:

1. A system comprising:

a first and second set of plurality of nodes;

a first bus associated with and connecting said first set of plurality nodes;

a second bus associated with and connecting said second set of plurality of nodes;

each node except one of each of said first and second sets of plurality of nodes including a processing unit, a memory, a bus coupled to the processing unit and memory, and a sensor means for sensing a write from the processing unit to the memory and for transmitting the sensed write including data and an address to which said data is being written on said associated bus without intervention of the processing unit;

fiber optic means for optically transmitting data and associated addresses from one excepted node to the other excepted node;

the excepted node of the first set of plurality of nodes including first converter means connected to the first bus for (1) receiving data and associated addresses on said first bus in a parallel fashion, (2) converting said data to corresponding optical signals, (3) transmitting said optical signals via said fiber optic means, (4) receiving optical signals from said fiber optic means in a serial fashion, and (5) transmitting the optical signals received from said fiber optic means onto said first bus, said first converter means including latches receiving and outputting data from said first bus or said fiber optic means in a parallel fashion and receiving and outputting diagnostic data in a serial fashion;

the excepted node of the second set of plurality of nodes including second converter means connected to the second bus for (1) receiving data and associated addresses on said second bus in a parallel fashion, (2) converting said data to corresponding optical signals, (3) transmitting said optical signals via said fiber optic means, (4) receiving optical signals from said fiber optic means in a serial fashion, and (5) transmitting the optical signals received from said fiber optic means onto said second bus, said second converter means including latches receiving and outputting data from said second bus or said fiber optic means in a parallel fashion and receiving and outputting diagnostic data in a serial fashion; and

both said first and second converter means including selection means for accepting for transmission only data having preselected associated addresses.

Term	Documents
SERIAL	196207
SERIALS	144
PARALLEL	1270750
PARALLELS	9397
CONVER$	0
CONVER	1873
CONVERA	1
CONVERABILITY	1
CONVERABLE	3
CONVERADAPTERACCESSKEY	1
CONVERAENCE	1
(L1 AND (SERIAL WITH PARALLEL WITH CONVER$)).USPT.	1

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Display Format: KWIC Change Format

Previous Page Next Page Go to Doc#

micro proces

L8: Entry 1 of 1 File: USPT Aug 6, 1996

DOCUMENT-IDENTIFIER: US 5544319 A
TITLE: Fiber optic memory coupling system with converter transmitting and receiving bus data in parallel fashion

Detailed Description Text (6):
The FMC 1 consists of four main sections: the memory coupled system 5 interface, the data paths (Rx and Tx) 7 and 8, the high speed serial data link interface 4, and the microprocessor. These areas are delineated using dashed lines in the functional block diagram (FIG. 2). The Fiber Transition Module (FTM) connects to the FMC high speed serial link interface. The FTM is a known and conventional piece of hardware and serves to connect the electrical signals to corresponding light signals and vice versa.

Detailed Description Text (19):
The FMC Rx and Tx data paths 7 and 8 move data between the MCS interface and the high speed serial data link. They also interface to the microprocessor allowing asynchronous data, interrupt transfers and flow control information to move between clusters.

Detailed Description Text (27):
The FMC microprocessor has the ability to interject data into and remove data from both the Tx and Rx data paths 7 and 8. Such data is referred to as control data to distinguish it from memory write transfers. General purpose async data, MCS-II multidrop console async data and interrupt pulses are all treated as control data.

Detailed Description Text (36):
An important feature of the FMC design, particularly from a diagnostic perspective, is that the latches in each quadrant can be accessed in both a parallel and serial fashion. During normal operation of the FMC, data moves through the latches using the parallel interface. The alternate serial interface allows the microprocessor on the FMC to shift data serially into and out of the latches.

Detailed Description Text (39):
The destination of the MC transfer is determined by the parity and address checks, the hit bit, and the flag bits received with the transfer. If any of the most significant four address bits is non-zero, the transfer is discarded. If the received parity does not equal the computed parity, the transfer is clocked into the microprocessor interface FIFO 21. The transfer is also placed into the micro FIFO if the parity is good but the flag bits indicate a control type transfer (which only occurs in the MCS hub). The destination of a memory write type transfer with good parity depends on the setting of the hit bit. If the hit bit is reset, the transfer is simply discarded. If the hit bit is set, the memory data, translated memory address and flag bits are clocked into the Tx FIFO 14.

Detailed Description Text (40):
The contents of the hit/translation RAM 12 are initialized by the FMC microprocessor. To change a location in the RAM 12, the microprocessor first puts the new value into the loading buffers 24. The microprocessor then causes GLOBAL BUSY to be asserted on the MC bus and waits long enough for any transfer in

progress to pass through the MC input latch 10. Then, the microprocessor causes the hit/translation RAM 12 to be written with the value from the loading buffers. GLOBAL BUSY is subsequently deasserted.

Detailed Description Text (42):
The micro interface 21 is only used when a FMC in a FOMCS hub needs to distribute interrupt, async of other control information to the other FMCs in the hub. If control busy is not asserted on the hub bus, the micro interface logic 21 requests use of the MC output latch 9. When the latch 9 is available, the control data is serially shifted into the latch 9. Odd parity for the transfer is computed by the microprocessor and shifted into the latch 9 following the data.

Detailed Description Text (43):
FIG. 9 shows a detailed view of quadrant 2. Processing begins in quadrant 2 when the control logic detects that the Tx latches 18 and 20 are empty and finds that the Tx FIFO 14 is not empty or that the microprocessor has loaded the micro interface latch. If the micro latch has been loaded, the contents of the latch are transferred to the Tx latches 18 and 20. Of the 72 bits transferred from the micro latch, 64 are also clocked into a pair of EDC (error detection code) generators 16a and 16b. The generated eight bit EDC and the 72 bits from the micro latch are clocked into the Tx latches 18 and 20. The contents of the Tx latches 18 and 20 are then passed to the high speed link serial transmitter 22 in two 40 bit transfers.

Detailed Description Text (49):
FIG. 11 shows a block diagram of the AMD 29818 latch used to implement the MC input and output latches 9 and 10 and the Rx latches 15 and 17 and Tx latches 18 and 20 on the FMC. In the FMC design, the normal data path through these latches is the parallel one from the D input through the pipeline register 29 to the Q output. The alternate serial path is accessible by the FMC microprocessor and is primarily used for diagnostic purposes. Note that the mux 30 (which is controlled by the MODE signal) allows either the contents of the shadow register 31 or the D input to serve as the input for the pipeline register 29. Also, note that the output of the pipeline register 29 is feed back into the shadow register 31. Thus, with appropriate hardware control, data can enter the latch in serial and exit in parallel or enter parallel and exit in serial.

Detailed Description Text (50):
These features are exploited by the FMC design which allows the microprocessor to serially load a latch in one quadrant, move the data along the normal parallel path from that latch to a latch in another quadrant and then serially read the contents of the destination latch. By comparing the data loaded into the first latch with that read back from the second, the microprocessor can determine if the data path is functional.

Detailed Description Text (78):
A Motorola 68000 microprocessor on the FMC provides the configuration system interface as well as data management for all transfers other than memory write transfers. This includes all asynchronous data, interrupts and error logging. It also provides diagnostic capabilities driven through the configuration programming interface.

Detailed Description Text (116):
Another usage of the microprocessor is to allow diagnosis of an individual FMC and/or high speed serial link without bringing the entire MCS network offline. This capability is particularly useful in the star network environment where it is undesirable to shut down the entire hub just to diagnose a problem between the hub and a particular cluster. If the problem turns out to be the high speed link or the FMC in the cluster, it can be corrected without taking down the entire hub. Of course, software resynchronization will probably be necessary between the affected cluster and the other clusters it was communicating with but the rest of the

clusters connected to the hub can continue to communicate without interruption.

Previous Doc Next Doc Go to Doc#